ABSTRACT OF THE DISCLOSURE

A compiler in which pseudo C descriptions (1) that are capable of describing parallel operations at a statement level and at a cycle precision by clock boundaries and register assignment statements are input, the register assignment statements are identified (S2), so as to generate executable C descriptions (3), to extract state machines having undergone reductions in the numbers of states, and to decide whether or not a loop to be executed in the 0th cycle is existent (S5), and if the loop is nonexistent, circuit descriptions (4) that are capable of being logically synthesized are generated. Thus, the pseudo C descriptions in which the clock boundaries are explicitly inserted into the C descriptions are input, and the pseudo C descriptions which permit the register assignment statements to be described in parallel at the statement level are input, so that a pipeline operation attended with a stall operation can be represented.